B.Sc.23132 - Electronics-II (Digital Electronics - I) Paper- II

P. Pages : 2

Time : Three Hours

2043

GUG/S/16/3337

Max. Marks : 50

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Notes : 1. All questions are compulsory and carry equal marks.
2. Draw neat and labelled diagrams wherever necessary.
3. Use of log table and calculator are allowed.

1. **Either**

a) For the given logic equation $f(A, B, C) = ABC + B\overline{C}D + \overline{A}BC$ **5**

   i) Draw a truth table
   ii) Simplify using k-map

   For the given logic equation $f(A, B, C, D) = \pi M(0, 1, 6, 7, 8, 11, 12, 14, 15)$ **5**

   i) Write the logic equation in POS form
   ii) Simplify using k-map

OR

b) What is demultiplexer ? Explain the operation of 1:4 DEMUX. using basic gates. Design 1:8 DEMUX using 1:4 DEMUX. **6+4**

2. **Either**

a) What is encoder? **2+8**
   Draw the logic diagram of decimal to BCD encoder & explain its working with truth table.

OR

b) What is half adder? Explain it with logic diagram and truth, table. **5+5**
   Draw the logic diagram of 4 bit binary adder. Explain its working.

3. **Either**

a) What is meant by clocked flip flop? Explain the working clocked SR FF. Also draw the timing diagram. **10**

OR

b) What is the main disadvantage of JK FF? How is it overcome in JKMS FF? Explain. **10**
   What is toggle flip flop? State its application.

4. **Either**

    a)   What is meant by modulus of a counter? How the required number of flip flops are calculated in modified counter. Draw the logic diagram of 4 bit down counter and explain its working. Write the count sequence and draw the timing diagram.   **10**

<div align="center">OR</div>

    b)   How many flip flops are required for mod 9 counter?   **2+8**
           Design and explain the mod-8 up synchronous counter. Write the count sequence for the counter.

5.   a)   What is Karnaugh map? Draw the two and four variable k-map.   **2½**

       b)   Explain 2 line to 4 line decoder.   **2½**

       c)   What is meant by: **2½**

           i)   Active high preset / clear inputs.

           ii)   Active low preset / clear inputs.

       d)   A synchronous counter is faster than an asynchronous counter. Justify the statement.   **2½**

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