S.Y.B.Sc.(Part-II)(With Credits)-Regular-Semester 2012 Sem IV

B.Sc.24132 - Electronics : Paper-II (Digital Electronics-II)

P. Pages : 1 **GUG/S/17/5603**

Time : Three Hours * 1 7 5 1 * Max. Marks : 50

Notes : 1. All questions are compulsory and carry equal marks.
2. Draw neat and well labelled diagram wherever necessary.
3. Use of log table/ Calculator is allowed.

1. **Either**

a) What are left shift and right shift registers? **2+6+2**
Explain the working of 4 bits right shift register and draw its necessary timing diagram. State any two applications of shift register.

OR

b) Explain the expansion of memory size on the basis of **8+2**
i) Word size, and
ii) Word capacity.
How many memory chips are required to design 2K bytes memory using 256 bytes of RAM chip.

2. **Either**

a) What are static and dynamic RAMs. **3+7**
Explain construction and working of static RAM. Cell

OR

b) Explain the basic structure of CCD. **3+5+2**
Explain the operation of CCD.
State its any two applications.

3. **Either**

a) What are D/A and A/D converters? **2+2+6**
Explain its need in digital systems.
Explain the working of weighted Resistor Ladder type D/A converter.

OR

b) What are drawbacks associated with a weighted resistor ladder? **3+1+6**
How are they removed in R-ZR ladder type D/A converter?
Explain working of R-2R ladder type D/A converter.

4. **Either**

a) Draw block diagram of digital clock. **3+7**
Explain its principle and working.

OR

b) Draw the block diagram of counter type A/D converter. **3+7**
And explain its construction and working.
Draw its timing diagrams.

5. a) What is buffer register? Explain. **2½ x 4**
b) Draw diagram of MOS RAM Cell and explain its working.
c) What will be the output voltage of a 4 bit R-2R ladder for binary input of 1101.
Given logic 0 = 0V, Logic 1 = 8V
d) Explain the use and working of sample and hold circuit.

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