S.Y. B.Sc. Semester – IV : B.Sc.24132

Electronics - II (Digital Electronics - II)

Paper - II

P. Pages : 3

Time : Three Hours Max. Marks : 50

Notes : 1. All questions are compulsory.
2. Each questions carry equal marks.
3. Draw neat diagram wherever necessary.
4. Use of log table/calculator is allowed.

1. Either

a) Explain with the help of logic diagram, the working of the 4-bit SISO shift register along with the timing diagram. How are memories classified on the basis of media, speed and data storage capacity. **5+5**

OR

b) Explain the working and importance of controlled 4-bit buffer register, A RAM chip of 256 byte capacity is available. How many chips are needed to obtain a memory of 2K bytes? Draw its necessary diagram **5+5**

2. Either

a) Explain the construction and working of bipolar RAM cell. **5+5**
Explain the operation of charge coupled device (CCD)

OR

b) Explain construction and working of diode matrix ROM. **5+5**
Explain the need and function of an on-chip decoding in a memory.

3. Either

a) Explain the working of a 4-bit weighted resistor type D/A converter. **6+2+2**
State its drawbacks.
How can it be improved by using op-amp.

OR

b) Explain the working of 4-bit R – 2R ladder type D/A converter with suitable diagram. **6+4**
What will be the output voltage of 4-bit R – 2R ladder corresponding to the binary inputs i) 1010 ii) 0101, where logic '0' = 0V and logic '1' = 8V?

4. a) State the principle and explain the working of a single slope A/D converter. Explain the working of successive approximation A/D converter with suitable diagram. **6+4**

OR

b) Draw the block diagram of dual slope type ADC. Explain its working alongwith timing diagram. Give the advantages and disadvantages of dual slope A/D converter. **2+5+3**

5. a) Explain with the help of logic diagram, the working of the 4-bit shift left register. **2.5**

b) Explain difference between static and dynamic RAM cell. **2.5**

c) Explain the need of ADC and DAC in electronic instrumentation system. **2.5**

d) Draw the block diagram of digital clock. **2.5**

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