

B.Sc. (With Credits)-Regular-Semester 2012 Sem V

B.Sc.3516 Electronics I (Microprocessor, Interfacing & PPI Devices) Paper- I (Compulsory)

P. Pages: 4

Time: Three Hours Max. Marks: 50

- Notes: 1. All questions are compulsory and carry equal marks.
 - 2. Draw a diagram wherever necessary.
 - 3. Use of log table / calculator is allowed.

1. **EITHER**

- a) Draw a block diagram of 8085 5 microprocessor and explain register array in it.
- b) Explain the function of following flags:-5
 - i) Carry status (CS)
 - ii) Auxiliary carry (AC)
 - iii) Zero flag (Z)
 - iv) Parity flag (P)
 - v) Sign flag (S)

OR

C	What is an instruction? Explain 1 byte,		
	2 byte and 3 byte instructions with		
	examples.		
d) Define :	5	
	i) fetch cycle		
	ii) machine cycle		
	iii) T-states		
	iv) opcode		
	v) operand		
E	ITHER		
a	, ,	5	
	register indirect and implicit addressing		
	mode with suitable examples.		
		_	
b	Explain the meaning of following	5	
	instructions:		
	i) MOV M, A		
	ii) MVI A, O5 H		
	iii) SBB r		
	iv) ADD B		
	v) ADI, data		
,	OR	_	
C		5	
	8085 with one example of each.		

2.

	d)	Write an ALP program to perform multiplication of any two 8-bit numbers.	5		
3 .	EITHER				
	a)	What is the need of interfacing? Explain with suitable example.	5		
	b)	Explain:	5		
		i) Memory mapped I/O scheme.			
		ii) I/O mapped I/O scheme.			
		OR			
	c)	Explain the synchronous and	5		
		asynchronous data transfer scheme in microprocessor.			
	d)	Explain the burst mode and cycle	5		
		stealing in DMA data transfer scheme.			
4.	Εľ	ГНЕК			
	a)	Explain the block diagram of 8255 PPI.	5		
	b)	Explain BSR mode and I/O mode of 8255 PPI. OR	5		
		On			

	c)	Explain the control word format of 8253 Interval timer.	5
	d)	Explain the operation of Intel 8253 in mode 0 and mode 1.	5
5 .	a)	Explain data, address and control bus.	21/2
	b)	Explain JMP instruction in $8085~\mu p$.	21/2
	c)	Explain interrupt driven data transfer scheme.	21/2
	d)	Draw a schematic diagram of Intel 8257 DMA controller.	21/2
